In the Claims

CLAIMS

Claims 1-41 (Canceled).

42. (Currently amended) A semiconductor assembly, comprising:

a semiconductor substrate having a pair of electrical nodes supported thereby; the electrical nodes being a first electrical node and a second electrical node, respectively, and at least one of the first and second electrical nodes having a lateral width defined by a pair of isolation regions formed within the semiconductor substrate on opposite sides of the at least one of the first and second electrical nodes;

an insulative mass over the substrate; the mass having a pair of openings extending therethrough to the electrical nodes; the individual openings each having a periphery defined by a bottom and at least one sidewall; the opening extending to the first electrical node being a first opening, and the opening extending to the second electrical node being a second opening;

a dielectric material layer within the openings; the dielectric material layer lining the at least one sidewall and bottom of the first opening, and lining the at least one sidewall but not a predominant portion of the bottom of the second opening;

conductive material plugs within the openings; the conductive material plug within the first opening being a first material plug, and the conductive material plug within the second opening being a second material plug; the first and

second conductive material plugs comprising the same chemically constituencies as one another;

the first electrical node, dielectric material within the first opening, and first conductive material plug together being incorporated into an anti-fuse construction; and

the second electrical node, dielectric material within the second opening, and second conductive material plug together being incorporated into an electrically conductive interconnect construction.

43. (Original) The assembly of claim 42 wherein the dielectric material layer comprises silicon nitride.

44. (Original) The assembly of claim 42 wherein the both conductive plugs are formed by common and simultaneous processing.

45. (Original) The assembly of claim 42 wherein the dielectric material is formed within the pair of openings by common and simultaneous processing.

46. (Original) The assembly of claim 42 wherein the dielectric material layer comprises silicon nitride and has a thickness of from about 30Å to about 100Å.

47. (Original) The assembly of claim 42 wherein the first electrical node comprises a p-type doped diffusion region within a semiconductive material of the semiconductor substrate.

48. (Original) The assembly of claim 42 wherein the first electrical node comprises an n-type doped diffusion region within a semiconductive material of the semiconductor substrate.

Claims 49-52 (Cancelled).

53. (Original) The assembly of claim 42 wherein the conductive plugs comprise conductively doped silicon.

54. (Original) The assembly of claim 42 wherein the conductive plugs comprise a metal.

55. (Original) The assembly of claim 42 wherein the conductive plugs comprise tungsten.

56. (Original) The assembly of claim 42 wherein the conductive plugs comprise copper.

57. (Original) The assembly of claim 42 wherein the conductive plugs comprise aluminum.

58. (Original) The assembly of claim 42 wherein the conductive plugs comprise copper and aluminum.

59. (Original) The assembly of claim 42 wherein the conductive plugs comprise a layer of titanium nitride against the dielectric material; and a mass of tungsten over the layer of titanium nitride.

60. (New) The assembly of claim 42 wherein the pair of the isolation regions comprise a chemical constituency that is different from a chemical constituency of the insulative mass.

61. (New) The assembly of claim 42 wherein the pair of the isolation regions comprise a pair of shallow trench isolation regions.

62. (New) A semiconductor assembly, comprising:

a semiconductor substrate having an upper surface and a pair of electrical nodes supported over and against the upper surface; the electrical nodes being a first electrical node and a second electrical node, respectively;

an insulative mass over the substrate; the mass having a pair of openings extending therethrough to the electrical nodes; the individual openings each having a periphery defined by a bottom and at least one sidewall; the opening extending to the first electrical node being a first opening, and the opening extending to the second electrical node being a second opening;

a dielectric material layer within the openings; the dielectric material layer lining the at least one sidewall and bottom of the first opening, and lining the at least one sidewall but not a predominant portion of the bottom of the second opening;

conductive material plugs within the openings; the conductive material plug within the first opening being a first material plug, and the conductive material plug within the second opening being a second material plug; the first and second conductive material plugs comprising the same chemically constituencies as one another;

the first electrical node, dielectric material within the first opening, and first conductive material plug together being incorporated into an anti-fuse construction; and

the second electrical node, dielectric material within the second opening, and second conductive material plug together being incorporated into an electrically conductive interconnect construction.

63. (New) The assembly of claim 62 wherein the first electrical node comprises a metal.

64. (New) The assembly of claim 62 wherein the first electrical node comprises copper.

65. (New) The assembly of claim 62 wherein the first electrical node comprises aluminum.

66. (New) The assembly of claim 62 wherein the first electrical node comprises copper and aluminum.